

REMARKS**BEST AVAILABLE COPY**

This application has been carefully reviewed in light of the Office Action dated October 1, 2002. Claims 1, 3-11, 25, 27-32, and 39 are pending in the present application. Applicant respectfully requests reconsideration of the above-referenced application in light of the following remarks.

Claims 1, 3-4, 9-10, 18, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 11 of Chiang et al. (U.S. Patent No. 5,739,579) ("Chiang") in view of Fig. 9 of Chiang. This rejection is respectfully traversed.

The Office Action contends that Fig. 11 discloses Applicant's invention except for a first and second conductor layer. To rectify this deficiency, the Office Action asserts that Fig. 9 of Chiang teaches a first and second conductor layer. However, it is illogical to combine Chiang's Fig. 9 with Fig. 11.

Chiang discloses multiple embodiments through Figures 1-25. If Chiang renders Applicant's invention obvious as asserted, Chiang would teach or suggest in an alternate embodiment a first and second conductor layer with a conductive plug comprising a single conductive material. Chiang simply does not teach or suggest this. In fact, Fig. 11 is an alternative embodiment of Chiang's invention which only teaches and suggests a single conductor layer provided with a single conductive plug. Fig. 11 specifically discloses an using aluminum as the interconnect material with the associated structure (Col. 11, lines 19-21). No other structure is suggested or contemplated. Moreover, the fact that Fig. 11 is a different embodiment from Fig. 9 would not suggest that the different embodiments be combined. Clearly, the Fig. 9 and 11 embodiments are combined in the rejection using impermissible hindsight.

The Office Action further argues that "[i]t is conventional to use copper with a barrier layer as a conductive interconnection layer instead of aluminum because copper has a lower resistivity than aluminum so as providing a higher speed." (Office Action, page 3).

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However, Chiang's Fig. 11 discloses a conductive plug comprising only tungsten (Col. 11, lines 24-25). Chiang teaches that "tungsten . . . [has] higher resistivities compared to aluminum, copper, gold, and silver." (Col. 2, lines 40-43) (emphasis added). If providing a lower resistivity and higher speed is conventional in integrated circuits, one skilled in the art would not combine Fig. 11 and Fig. 9 of Chiang, since Fig. 11 of Chiang utilizes tungsten as a conductive plug, which would increase the total resistivity.

Claims 3-4, and 9-10 depend from and contain all of the limitations of claim 1. Accordingly, claims 3-4 and 9-10 are allowable for at least the reasons set forth above for allowance of claim 1.

Claims 5-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Wang et al. (U.S. Patent No. 6,184,128) ("Wang"). Claims 5-6 depend from and contain all of the limitations of claim 1. Accordingly, claims 5-6 are allowable for at least the reasons given above for allowance of claim 1.

Claims 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Hong et al. (U.S. Patent No. 6,008,117) ("Hong"). Claims 7-8 depend from and contain all of the limitations of claim 1. Accordingly, claims 7-8 are allowable for at least the reasons given above for allowance of claim 1.

Claims 11, 15-17, 25, 27, 30-32, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 11 of Chiang in view of Fig. 9 of Chiang and further in view of Matsuura (U.S. Patent No. 5,598,027).

As discussed above, Chiang does not disclose or suggest a structure with two conductive layers over a plug formed of a single conductive element as recited by claims 11 and 25.

Further, the combination of Matsuura and Chiang is improper. There is no motivation to have a first and second etched via over a single conductive plug. Chiang

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teaches that “[i]n contrast to the prior art, the interconnects of the present invention can be the same width.” (Col. 10, lines 36-37). Still further, Chiang discloses that the prior art taught interconnects that must be wider than the contact plug’s width which “consumes a considerable amount of area on the chip.” (Col. 10, lines 29-30). Forming interconnects that are the same width as the conductive plug is an important feature of Chiang.

Chiang discloses interconnect channels such as opening 330 (FIG. 16), opening 353 (FIG. 20), and interconnect channel 351 (FIGS. 21, 22), all of which are openings possessing a single diameter. Matsuura provides vias B and C possessing different diameters. Accordingly, there is no motivation to use Matsuura’s wider interconnects with Chiang.

Claims 15-17 depends from and contains all of the limitations of claim 11, and claims 27, 30-32, and 39 depend from and contain all of the limitations of claim 25. Accordingly, claims 15-17 are allowable for at least the reasons set forth above for allowance of claim 11, and claims 27, 30-32, and 39 are allowable for at least the reasons set forth above for allowance of claim 25.

Claims 13-14 and 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Matsuura. Claims 13-14 depend from and contain all of the limitations of claim 11. Similarly, claims 28-29 depend from and contain all of the limitations of claim 25. Accordingly, claims 13-14 and claims 28-29 are allowable for at least the reasons given above for allowance of claims 11 and 25 provided above.

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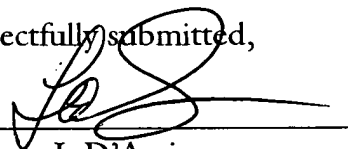
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There are several important features of claims 1, 3-11, 13-17, 25, 27-32, and 39 that are not taught anywhere in the cited prior art. Accordingly, the rejection of claims 1, 3-11, 13-17, 25, 27-32, and 39 should be withdrawn. Allowance of the application with claims 1, 3-11, 25, 27-32, and 39 is respectfully solicited.

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Respectfully submitted,

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